Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A computer system comprising:

a processor for controlling operations of the computer system;

a bus coupled to the processor; and

an interface device, coupled to the processor through the bus, comprising:

a first controller for performing a first logic operation; and

a second controller coupled to the first controller for performing a second logic operation;

wherein when the processor initializes the apparatus, the first controller responds with a message to the processor to indicate that the apparatus is a single-function device and the second controller is disabled,

wherein the first controller determines which one of the first controller and the second controller responds to the processor according to a command from the processor.

[c2] 2.The computer system of claim 1, wherein the interface device comprises:

a selecting module coupled to the second controllers for

allowing either the first controller or the second controller to utilize the bus;

3.The computer system of claim 1, wherein the first controller comprises:

a register for storing a flag used to control whether either the first controller or the second controller is enabled.

[c3] 4.The computer system of claim 1, wherein the interface device is a PCI interface device and the bus is a PCI bus.

[c4] 5.The computer system of claim 1, wherein when the processor initializes the interface device, the first controller responds with a message to the processor to request a total memory volume including a first portion that will be utilized by the first controller and a second portion that will be utilized by the second controller.

[c5] 6. The computer system of claim 1, wherein the interface device further comprises:

a third controller coupled to the first controller for performing a third logic operation;

7. The computer system of claim 1, wherein the interface device further comprises:

a third controller coupled to the second controller for performing a third logic operation;

8.An apparatus coupled to a processor through a bus,

the apparatus comprising:

a first controller for performing a first logic operation, wherein when the processor initializes the apparatus, the first controller responds with a message to the processor to indicate that the apparatus is a single-function device; and

a second controller coupled to the first controller for performing a second logic operation, wherein when the processor initializes the apparatus, the second controller is disabled;

wherein the first controller determines which one of the first controller and the second controller responds to the processor according to a command from the processor.

[c6] 9.The apparatus of claim 8, further comprises:

a selecting module coupled to the first and second controllers for allowing either the first controller or the second controller to utilize the bus;

10. The apparatus of claim 9, wherein the selecting module is within the first controller.

[c7] 11.The apparatus of claim 9, wherein the first controller comprises:

a register for storing a flag used to control the operation of the selecting module.

[c8] 12.The apparatus of claim 8, wherein the first controller

comprises:
a register for storing a flag used to control whether either the first controller or the second controller responds to the processor.

[c9] 13. The apparatus of claim 12, wherein the flag is changed by the processor.

[c10] 14The apparatus of claim 9, wherein the bus is a PCI bus and the first controller further comprises:
a first INTB pin, a first REQB pin, a first GNTB pin, and a first IDSEL pin, all coupled to the PCI bus.

[c11] 15.The apparatus of claim 14, wherein each of the controllers further comprises:
at least a plurality of address pins, a Frameb pin, an Irdyb pin, and a Trdyb pin, all coupled to the selecting module, wherein the address pins, the Frameb pin, the Irdyb pin, and the Trdyb pin are in accordance with the PCI specification.

[c12] 16.The apparatus of claim 8 wherein when the processor initializes the apparatus, the first controller responds with a message to the processor to request a total memory volume including a first portion that will be utilized by the first controller and a second portion that will be utilized by the second controller.

[c13] 17.A method for using a bus in the computer system which comprises a processor and an interface device, the interface device comprising a first controller and a second controller, and being coupled to the processor through the bus, the method comprising:
generating a first message to indicate that the interface device is a single-function device when the interface device is initialized;
generating a second message to request a total memory volume including a first portion that will be utilized by the first controller and a second portion that will be utilized by the second controller; and
determining which one of the first controller and the second controller responds to the processor according to a command from the processor.

[c14] 18.The method of claim 17 further comprising:
using a flag stored in a register of the first controller to control whether either the first controller or the second controller responds to the command.

[c15] 19.The method of claim 18 wherein the flag is changed by the processor.

[c16] 20.The method of claim 18 wherein further comprising:
disabling the second controller when the interface device

is initialized.